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1    Method And Apparatus For Adapting An Information Carrying2    Signal

3

4    This invention relates to the field of communications  
5    systems. More particularly, this invention relates to a  
6    method and apparatus for adapting an information carrying  
7    signal. The method and apparatus can be readily employed  
8    within a transmitter of a communication system so as to  
9    overcome signal impairment effects within the system.  
10   The invention has particular use as an equalisation  
11   element in the field of fibre optic communications  
12   networks to counteract dispersion and other complex  
13   signal impairments.

14

15

16    Background Art

17

18   Electronically adjustable equalization transmitter  
19   schemes for communications systems are well known in the  
20   art. Such a scheme is embodied in US Patent No. US  
21   6,393,062 entitled "Methods and circuits for generating a  
22   pre-emphasis waveform". This scheme relies on pre-  
23   compensating a waveform by selectively boosting the  
24   electronic signal to a value larger than the nominal

1 signal, essentially providing data-dependant pulse  
2 amplitude modulation.

3

4 There are however several major drawbacks with this  
5 scheme. In the first instance pulse amplitude modulation  
6 is not a suitable control method for increasing the  
7 optical intensity in order to provide compensation in an  
8 optical fibre system because:

9 a) in standard systems amplitude information is  
10 removed using a pre-laser limiting or clipping  
11 function in order to simplify driver electronics;  
12 and

13 b) lasers are very non-linear devices and so  
14 amplitude modulation is non-linearly related to  
15 optical intensity.

16

17 As a result lasers do not respond or do not respond well  
18 to pulse amplitude modulation.

19

20 Secondly, with higher data-rate signals, for example  
21 greater than 10 Gbps, such a scheme is very difficult to  
22 practically implement in a low cost electronic CMOS or  
23 BiCMOS silicon technologies as the required switching  
24 speeds and slew rates will be unwieldy and difficult to  
25 control accurately.

26

27 A further drawback is that the amplitude and settling  
28 characteristics relied upon to perform the equalisation  
29 are subject to unacceptable variations and so are not  
30 suitable for precision or high speed applications. As  
31 shown in a particular embodiment, the scheme requires  
32 additional circuitry to accurately control the amount of  
33 boost which in-turn increases complexity, power and cost  
34 of the system.

1  
2 Furthermore, the signal boosting scheme described  
3 requires the driving of a larger than normal signal.  
4 This may not always be possible given power supply  
5 constraints or, conversely, requires some signal  
6 amplitudes to be reduced, which does not maximise  
7 available signal to noise available for these signals.

8

9 European Patent Application No. EP 0,884,867 describes a  
10 system for "Equalization, pulse shaping and regeneration  
11 of optical signals". In particular this document teaches  
12 of an equalisation arrangement for use in optical systems  
13 with optical fibre media. The scheme relies on  
14 equalisation using weighted tap filters crafted so as to  
15 employ optical components in the optical domain. Such an  
16 approach again exhibits several inherent disadvantages.

17

18 Firstly, such equalisation can only compensate for linear  
19 effects that contribute to Inter-Symbol-Interference  
20 (ISI) such as those caused by dispersion. However, other  
21 non-linear effects including laser and fibre chirp,  
22 changes in fibre characteristics with optical intensity,  
23 duty cycle distortions and unequal rise/fall times of the  
24 transmitter or receiver are not addressed.

25

26 Secondly, the system is relatively expensive to make as  
27 it relies on several expensive optical amplifiers,  
28 optical monitors and customised and precise lengths of  
29 delay matched optical fibres.

30

31 Thirdly, the physical size and inherent power  
32 requirements make such schemes less desirable or  
33 practical in modern installations.

34

1 It is an object of an aspect of the present invention to  
2 provide a method and apparatus for filtering an  
3 information carrying signal. In particular this method  
4 and apparatus can be employed for equalisation of the  
5 information carrying signal so as to overcome the  
6 problematic features of the prior art.

7

8

9 **Statements of Invention**

10

11 According to a first aspect of the present invention  
12 there is provided a method of adapting an information  
13 carrying signal that comprises a plurality of data pulses  
14 that exhibit a range of pulsedwidths and which are  
15 generated by a transmitter for transmission through a  
16 propagation medium, the method comprising the step of  
17 introducing one or more sub-pulses to one or more of the  
18 plurality of data pulses prior to the information  
19 carrying signal entering the signal propagation medium  
20 wherein a pulsedwidth of each of the one or more sub-  
21 pulses is less than a minimum pulsedwidth of the plurality  
22 of data pulses.

23

24 The introduction of the one or more sub-pulses whose  
25 pulse width is less than the minimum pulse width of the  
26 plurality of data pulses allows for the energy contained  
27 within the plurality of data pulses to be altered thus  
28 providing a means for the information carrying signal to  
29 be controllably adapted.

30

31 Most preferably an amplitude of the one or more sub-  
32 pulses is of an opposite sign to an amplitude of an  
33 associated data pulse.

34

1  
2 Preferably the introduction of one or more of the sub-  
3 pulses are timed so that these sub-pulses are contained  
4 within one or more of the plurality of data pulses to  
5 which the sub-pulses are introduced.

6  
7 Preferably the introduction of one or of the more sub-  
8 pulses are timed so that these sub-pulses coincide with  
9 one or more edges of one or more of the plurality of data  
10 pulses to which the sub-pulses are introduced.

11  
12 Preferably, the one or more sub-pulses are introduced to  
13 one or more of the plurality of data pulses when the data  
14 pulse exhibits a pulselength above a first predetermined  
15 pulselength of the plurality of data pulses so as to  
16 provide a means for low frequency filtering the  
17 information carrying signal.

18  
19 Alternatively, the one or more sub-pulses are introduced  
20 to one or more of the plurality of data pulses when the  
21 data pulse exhibits a pulselength below a second  
22 predetermined pulselength of the plurality of data pulses  
23 so as to provide a means for high frequency filtering the  
24 information carrying signal.

25  
26 Most preferably the first predetermined pulselengths of  
27 the plurality of data pulses corresponds to the minimum  
28 pulselength of the plurality of data pulses so as to  
29 provide a means for equalising the information carrying  
30 signal.

31  
32 It is known that attenuation of a data signal is  
33 frequency or pulselength dependent i.e. the higher the  
34 frequency the greater the attenuation experienced. Thus

1 by employing the sub-pulses to effectively remove energy  
2 from the lower frequency components of the data signal  
3 equalisation of the data signal following transmission  
4 through a propagation medium is achieved.

5

6 Preferably the timing of introducing the one or more sub-  
7 pulses to one or more of the plurality of data pulses is  
8 variable.

9

10 Most preferably, the number of sub-pulses introduced is  
11 directly dependent upon the pulselwidth of the associated  
12 data pulse. Alternatively, the pulselwidth of the one or  
13 more sub-pulses is directly dependent upon the pulselwidth  
14 of the associated data pulse.

15

16 Preferably the coinciding of the one or more sub-pulses  
17 with one or more edges of one or more of the plurality of  
18 data pulses acts to time shift a rising and/or a falling  
19 edge of an associated data pulse.

20

21 Optionally the time shifting of the rising and/or the  
22 falling edge of the associated data pulse is by a  
23 predetermined value. Alternatively, the time shifting of  
24 the rising and/or the falling edge of the associated data  
25 pulse is directly dependent upon the pulselwidth of the  
26 associated data pulse.

27

28 Preferably the time shifting of the rising edge of an  
29 associated data pulse comprises advancing in time the  
30 rising edge.

31

32 Preferably the time shifting of the falling edge of an  
33 associated data pulse comprises delaying in time the  
34 falling edge.

1 According to a second aspect of the present invention  
2 there is provided an electronic circuit suitable for  
3 adapting an electronic input signal of a transmitter, the  
4 electronic input signal comprising a plurality of  
5 electrical data pulses, the electronic circuit comprises  
6 an electronic input channel, a clock pulse phase delay  
7 circuit, a signal processor and an electronic output  
8 channel wherein the signal processor analyses one or more  
9 of the plurality of electrical data pulses supplied on  
10 the electronic input channel and one or more clock pulse  
11 phase delay signals provided by the clock pulse phase  
12 delay circuit so as to introduce one or more electrical  
13 sub-pulses to one or more of the plurality of electrical  
14 data pulses so as to provide an adapted electronic output  
15 signal on the electronic output channel.

16

17 Preferably the introduction of one or more of the  
18 electrical sub-pulses are timed so that these electrical  
19 sub-pulses are contained within one or more of the  
20 plurality of electrical data pulses to which the  
21 electrical sub-pulses are introduced.

22

23 Preferably the introduction of one or more of the  
24 electrical sub-pulses are timed so these electrical sub-  
25 pulses coincide with one or more edges of one or more of  
26 the plurality of electrical data pulses to which the  
27 electrical sub-pulses are introduced.

28

29 Most preferably the clock pulse phase delay circuit  
30 comprises means for supply a first clock pulse and one or  
31 more phase delayed clock pulses to the signal processor.

32

33 Preferably the signal processor comprises first  
34 electronic means for producing an internal signal pulse

1 when subsequent electrical data pulses exhibit  
2 substantially the same value.

3

4 Preferably the signal processor further comprises a  
5 second electronic means for introducing an electronic  
6 sub-pulse to the electronic input signal when the  
7 internal signal pulse is detected by the second  
8 electronic means.

9

10 Preferably the signal processor further comprises a third  
11 electronic means for altering the timing of the  
12 electrical sub-pulses so allowing the sub-pulses to  
13 coincide with a rising or falling edge of an electrical  
14 data pulse.

15

16 Most preferably the timing of the first electronic means  
17 is controlled by the first clock pulse.

18

19 Preferably the second and third electronic means are  
20 controlled by the combination of the first clock pulse  
21 and the one or more phase delayed clock pulses.

22

23

24 **Brief Description of Drawings**

25

26 In the following detailed description of the preferred  
27 embodiments or mode, reference is made to the  
28 accompanying drawings, which form part hereof, and in  
29 which are shown, by way of illustration, specific  
30 embodiments in which the invention may be practised. It  
31 is to be understood that other embodiments may be  
32 utilised and structural changes may be made without  
33 departing from the scope of the present invention.

34

1 FIGURE 1 shows a system block diagram of a typical  
2 communication channel that will be used for reference  
3 purposes;

4

5 FIGURE 2 shows a system block diagram of a typical long-  
6 haul fibre optic communication channel that incorporates  
7 an adaptable signal processing element, shown within the  
8 transmitter function, in accordance with an aspect of the  
9 present invention;

10

11 FIGURE 3 shows an example of a standard transmitted (in)  
12 and received (out) signal waveform before any wave signal  
13 processing in the transmitter is applied;

14

15 FIGURE 4 shows the resulting "eye diagram" of the  
16 information presented in Figure 3;

17

18 FIGURE 5 shows details of the operation of the adaptable  
19 signal processing element employed to equalise the  
20 received (out) signal waveform at the output of the  
21 transmitter and in particular schematically presents  
22 definitions of coefficient terms employed for achieving  
23 this result.

24

25 FIGURE 6 shows an example of a modified transmitted (in)  
26 and received (out) signal waveform after the adaptable  
27 signal processing element within the transmitter is  
28 applied;

29

30 FIGURE 7 shows the resulting improved "eye diagram" of  
31 the information presented in Figure 6;

32

1 FIGURE 8 shows a top level schematic view of the  
2 preferred embodiment of the adaptable signal processing  
3 element;.

4

5 FIGURE 9 shows detail of the clock pulse signal waveforms  
6 employed within the adaptable signal processing element  
7 such that it operates to equalise the received (out)  
8 signal waveform;

9

10 FIGURE 10 shows schematic detail of the signal processor  
11 apparatus; and

12

13 FIGURE 11 shows details of the waveforms generated within  
14 adaptable signal processing element of Figure 5.

15

16

17 **Detailed Description**

18

19 Adaptable schemes can be used in order to improve some  
20 desired metric of a communications system's performance.  
21 By improving the system performance an adaptable system  
22 allows higher bandwidth or higher data-rate or longer  
23 reach or more compact or less expensive systems to be  
24 made.

25

26 A detailed description of the method and apparatus for  
27 such an adaptable system shall now be described and in  
28 particular to its employment as an equaliser for an  
29 information carrying signal transmitted within an optical  
30 system. This equalisation can be used to counteract  
31 bandwidth limiting or other signal impairments within the  
32 channel.

33

1 Within a communications system typical signal impairment  
2 or degradation mechanisms include the rise time, fall  
3 time, bandwidth or other distortion of the receiver or  
4 transmitter, dispersion, chirp, reflection and bandwidth  
5 limitations within the media and interference from other  
6 signals. The words signal impairments or degradation  
7 mechanism will be used extensively throughout this  
8 document for any linear or non-linear, stationary or non-  
9 stationary or other non-ideal affect anywhere in the  
10 communications channel that causes the received signal to  
11 be adversely affected.

12

13 The resultant effects of these degradation mechanisms on  
14 the signal are often dependant on the inter-relationship  
15 of the signal being transmitted and the degradation  
16 mechanism itself. Within some bounds these are  
17 repeatable effects. These will be generally referred to  
18 as deterministic effects throughout this document.

19

20 The task of equalisation or compensation is to modify the  
21 physical characteristics of an information carrying  
22 signal in order to correct, accommodate or rectify some  
23 impairment in it. In an aspect of the present invention  
24 the equalisation is achieved by synthesising a new  
25 transmitted wave-shape using a high speed signal  
26 processor. This signal processing, synthesis and  
27 resultant equalisation is achieved using a technique  
28 whereby energy is added or subtracted to the wave shape  
29 in the form of constructive or destructive sub-pulses  
30 and/or by manipulating within the information carrying  
31 signal individual pulse edge positions. The method and  
32 apparatus for the preferred embodiment of this are as  
33 follows.

34

1 A typical one-way communications system is shown in  
2 Figure 1. The channel 6 transmits its input signal, in  
3 1, via the transmitter 2, through the media 3, to the  
4 receiver 4 and out in the form of output signal 5.

5

6 A typical long-haul fibre optic communication showing the  
7 preferred embodiment is shown in Figure 2. The  
8 transmitter 2 includes the adaptable signal processor 7  
9 that provides for wave synthesis equalisation in front of  
10 the optical source 8. The input signal 1, is modified by  
11 the action of the adaptable signal processor to produce  
12 the equalised electronic signal, ewave 25. The optical  
13 source converts the electronic signal into an equivalent  
14 optical signal, owave 26. The media 3, here an optical  
15 fibre, itself is shown partitioned into smaller lengths  
16 with optical amplifiers 11 used to boost the signal along  
17 the length, as is typical of these systems, in order to  
18 maximise transmission distances. Amplifiers or repeaters  
19 11 are optionally required as the signal 1 becomes  
20 attenuated with distance due to losses within the optical  
21 fibre 3. The optical signal 26 is received at the  
22 optical detector 9 and amplified to an electrical signal  
23 by the post amp 10.

24

25 Figure 3 shows the time-domain input and output waveforms  
26 of the entire communications system represented in Figure  
27 2 when the signal processing element 7 is disabled.. The  
28 figure shows the input signal waveform 1 and the modestly  
29 distorted output signal waveform 5 when no equalisation  
30 or other correction is employed. Note that the exact  
31 output waveform 5 is for illustrative purposes only and  
32 more or less complex distortion can occur, and for this  
33 purpose no random or further deterministic jitter is  
34 shown. The waveforms drawn illustrate a non return to

1 zero (NRZ) signalling scheme which is most likely  
2 implemented as a differential signal with the signal  
3 swinging above (positive) and below (negative) the zero  
4 axis. Where the signal is intended to be digital or  
5 binary in nature the signals may be alternatively  
6 represented by digital signals where a logical "one" is a  
7 differentially positive signal and a logical "zero" is a  
8 differentially negative signal.

9

10 Figure 4 shows an alternative and readily used time-  
11 domain representation of the output waveform 5 as  
12 described in Figure 3 and called an "eye-diagram". The  
13 purpose of the post receiving stage (not shown) is to  
14 determine the optimal sampling point, for example in the  
15 middle of the "eye" 14 and decide whether a "one" or a  
16 "zero" was sent. However making a decision on whether  
17 the signal should be a "one" or a "zero" is made more  
18 difficult by the data jitter 15 and eye closure 16. The  
19 jitter 15 increases and the eye closes 16 due to a number  
20 of impairment and degradation mechanisms. This commonly  
21 manifests itself as inter-symbol interference as  
22 neighbouring bit-patterns constructively or destructively  
23 interfere.

24

25 Figure 5 shows a definition of a new input waveform  
26 "wave", synthesised using the adaptable signal processor  
27 7. The top waveform 25 drawn illustrates the electrical  
28 signal, ewave 25, using a NRZ signalling scheme which is  
29 most likely implemented as a differential signal with the  
30 signal swinging above (+ve) and below (-ve) the zero  
31 axis.

32

33 Where the signal is intended to be digital or binary in  
34 nature the signals may be alternatively represented by

1 digital signals where a logical "one" is a differentially  
2 positive signal and a logical "zero" is a differentially  
3 negative signal.

4

5 The lower waveform in Figure 5 represents the resultant  
6 optical output, owave 26, generated by the optical source  
7 8. This waveform illustrates that the light is either on  
8 or off as controlled by the electronic signal ewave 25.  
9 Therefore, an important advantage of this scheme is  
10 clearly visible in that this scheme does not at all rely  
11 on any amplitude characteristic of the electronic signal  
12 ewave 25 or intensity response from the optical source 8  
13 to an electronic amplitude in order to achieve  
14 equalisation. This is important as the optical source  
15 driving electronics normally would contain a limiting  
16 amplifier and the optical source would be driven into a  
17 power maximum condition, rather than linearly controlled,  
18 as the source is extremely non-linear in nature.

19

20 Electronic signal ewave 25 shows all rising edges 19, or  
21 all falling edges 20 can be independently extended or  
22 reduced in time, represented by dTr 22 or dTf 21  
23 respectively, in order to alter the spatial zero crossing  
24 and by adding or reducing energy within the transmitted  
25 bit patterns. These altered pulse edges can therefore be  
26 employed to counter-act artefacts including edge  
27 distortion, non-linear rise fall times, duty cycle  
28 distortions and laser chirp.

29

30 In addition energy can be added to a transmitted "zero"  
31 by temporarily inverting the optical signal 30 so as to  
32 insert a short pulse of "one" 17, with duration dTl 23,  
33 and energy can be independently removed from a  
34 transmitted "one" by temporarily inverting the optical

1 signal 30 so as to inserting a small pulse of "zero" 18.,  
2 with duration dTh 24. This is a remedy for equalising  
3 modal, chromatic and polarisation distortion within the  
4 optical fibre or other bandwidth limitations. In so  
5 doing the adaptable signal processor 7 stops symbol  
6 dependant energy over-spill from one symbol to the next  
7 and minimises interference between symbols and removes  
8 ISI. The input waveform 1 is thus pre-distorted by the  
9 adaptable signal processor 7. This technique is most  
10 appropriate to optical systems because the optical source  
11 either usually incorporates a limiter function in the  
12 optical pre-drive circuitry or the optical source 8 is  
13 operated at near maximum photonic energy output or is so  
14 non-linearly compressed so as to act like a limiting  
15 function. It is therefore only the existence of the  
16 electronic signal ewave 25 above or below the zero-cross  
17 discrimination point and not the signal amplitude that  
18 warrants attention and suitably exploited when  
19 synthesising this equaliser.

20

21 Figure 6 shows the time-domain input and output waveforms  
22 in a communications system employing this invention. The  
23 figure shows the synthesised electronic signal ewave 25  
24 and the now less distorted output signal 5 after  
25 equalisation has been employed. Note this waveform 25 is  
26 for illustrative purposes only and no random jitter is  
27 shown and depending on the compensating parameters set  
28 the waveform can be more or less equalised.

29

30 Figure 7 shows the resulting improved "eye diagram" of  
31 the information presented in Figure 6. The job of the  
32 receiver 4 is made far easier because the data jitter 15  
33 (normally measured in ps) and the eye closure 16  
34 (normally measured in dBs) are greatly improved over that

1 presented in Figure 4. Hence the sampling point 14 is  
2 more easily obtained and tracked than that shown in  
3 Figure 4.

4

5 Figure 8 shows a preferred embodiment of a circuit  
6 schematic of the adaptable signal processor 7. It can be  
7 seen to comprise the input signal, in 1, and its  
8 synchronous clock "clk" signal 51 which are employed to  
9 produce output "ewave" signal 25 from a signal processor  
10 65. The apparatus shows four programmable time delay  
11 circuits dt1 52, dt2 54, dt3 56 and dt4 58. The time  
12 delay circuits produce four phases of "clk" 51, "clkp1"  
13 53, "clkp2" 54, "clkp3" 57 and "clkp4" 59 that are  
14 delayed but synchronous versions of "clk" 51. The time  
15 delay circuits are independently controlled by  
16 coefficient words Cp1 60, Cp2 61, Cp3 62 and Cp4 63. The  
17 coefficient words are stored in a register bank 64 that  
18 can be updated and refreshed as appropriate by a micro  
19 controller or such scheme. The time delay circuits 52,  
20 54, 56 and 58 can be readily implemented using, for  
21 example, unit delay cells, phase interpolation or delay  
22 locked loop techniques or any other scheme that allows a  
23 signal to be controllably delayed.

24

25 Figure 9 shows a particular electronic waveform 25  
26 generated by the adaptable signal processor 7 when  
27 employed in its preferred embodiment as an equalising  
28 element. Figure 9 further comprises schematic  
29 representations of the "clk" signal 51 and the four  
30 generated phases "clkp1" 53, "clkp2" 55, "clkp3" 57 and  
31 "clkp4" 59. It should be noted that the clocks shown are  
32 all shown at full rate, however similar schemes could be  
33 derived using sub-rate clocks without departing from the  
34 scope of this invention.

1

2 In particular:

3       • "clkp1" 53 rising marks the falling edge 20 of the  
4       "ewave" signal 25, and can be positioned to rise  
5       before or after the edge of the "clk" 51 signal  
6       thus supporting pre-emption or postponing of the  
7       falling edge 20;

8       • "clkp2" 55 rising marks the rising edge 19 of the  
9       "ewave" signal 25, and can be positioned to rise  
10      before or after the rising edge of the "clk" 51  
11      signal thus supporting pre-emption or postponing  
12      of the rising edge 19;

13      • "clkp3" 57 marks the leading edge of the inversion  
14      sub pulses 17 and 18 of the "ewave" signal 25; and

15      • "clkp4" 59 marks the trailing edge of the  
16      inversion sub pulses 17 and 18 of the "ewave"  
17      signal 25.

18

19 As the inversion pulses 17 and 18 are broadened by the  
20 action of the clocks so more energy is added or removed  
21 from the information carrying signal generated by the  
22 optical source 8. A second process for varying the  
23 energy within the information carrying signal is achieved  
24 by shifting in time the inversion sub pulses 18 and 19  
25 through the controlled operation of the clocks. These  
26 sub pulses can either be shifted in time towards a rising  
27 edge 19 or towards a falling edge 20 so that energy can  
28 be accurately removed or added to these edges as  
29 appropriate.

30

31 In a preferred embodiment the +ve sub pulse inversion 17  
32 and the -ve sub pulse inversion 18 are delimited by the  
33 same timing clock edges, namely "clkp3" 57 and "clkp4" 59.  
34 It will be appreciated by one skilled in the art that

1 this need not necessarily be the case and in other  
2 embodiments, the +ve and -ve inversion sub pulses, 17 and  
3 18, could be readily made independently controllable.  
4 This could be achieved via the incorporation of  
5 additional time delay elements so as to generate  
6 additional clocks and appropriate changes to the signal  
7 processor 65 in order to include this data dependency.

8

9 Further detail of the signal processing block 65 is  
10 presented in Figure 10. In summary:

- 11     • Elements "inv" 114, 116, 110 act to logically  
12         invert the signal between their input and their  
13         output values;
- 14     • Elements "buf" 115, 109 act to buffer the signal  
15         between their input and their outputs, often used  
16         as unit delay elements to match "inv" elements for  
17         timing purposes;
- 18     • Element "xor" 113 act to logically convert the  
19         signal between their input and their outputs, such  
20         that the output is only a logic high when one and  
21         only one input is logically high;
- 22     • Elements "and" 107, 111, 112 act to logically  
23         convert the signal between their input and their  
24         outputs, such that the output is only a logic high  
25         when both inputs are logically high; and
- 26     • Elements "latch" 100,101,102,103,104,105,106 act  
27         to logically convert the signal between their  
28         input and their outputs, such that the output is a  
29         copy of its input but delayed one clock cycle by  
30         the action of the respective clk so as to act as a  
31         memory element that latches its input to its  
32         output.

1 It will again be apparent to those skilled in the art  
2 that other elemental logical functions can be used to  
3 form equivalent logical functions within Figure 10  
4 without departing from the scope of this invention. It  
5 should also be noted that latch elements 100, 103 and 105  
6 are optional elements, and are incorporated for timing  
7 synchronisation purposes only.

8

9 The purpose of the logic elements indicated as Arm A 130  
10 is to produce a "pulse" signal 121. Figure 10 shows that  
11 the input signals to Arm A comprise the input signal "in"  
12 1 and the clock signal "clk" 51. A next sample output  
13 S(n) 122, a present sample output S(n+1) 123 and a  
14 previous sample output S(n+2) 124 are the outputs from  
15 the latches 100, 101 and 102, respectively in response to  
16 clock signal "clk" 51. The internal "pulse" signal 121  
17 is thus generated whenever two identical consecutive pre-  
18 ceding bits in S(n+1) 123 and S(n+2) 124 are detected,  
19 shown here generated by the "xor" function of element 113  
20 and inversion in "inv" 114 in order to produce the  
21 correct pulse signal 121.

22

23 The purpose of Arm C 132 is to produce a pulse' signal  
24 129 so providing a means for generating sub pulses 17 and  
25 18. Arm C 132 comprises elements 109 "buf" employed to  
26 provide a delay element to match that introduced by  
27 element "inv" 110. Element 111 "and" acts so as to  
28 create a shortened gating pulse pulse' 128 as defined by  
29 the edges of "clkp3" 57 and "clkp4" 59, and the  
30 coincidence of their high periods. The shortened pulse  
31 pulse' 129 is then produced from the output of element  
32 "and" 112 under the gating control of the internal pulse  
33 121 employed here as a control signal. The pulse' 129  
34 gating signal is therefore data dependant, as determined

1 by Arm A 130, and thus the sub pulse are data dependently  
2 controlled so as to either allow normal 17 or inverted 18  
3 sub pulses to be multiplexed by "mux" 108 onto on the  
4 electronic signal ewave 25. In so doing bit symbols can  
5 be temporarily inverted and electronic equalisation  
6 provided without any requirement for normal amplitude  
7 modulation techniques being employed to the optical  
8 signal 30.

9

10 The purpose of Arm B 131 is to produce an  $S(n+1)''$   
11 signal 127 and so provide a means for varying the rising  
12 19 and falling edges 20. Arm B 131 comprises latch  
13 elements 104 and 106 that act to transfer the data from  
14 the controlled phase delayed clock signals "clkp1" 53 and  
15 "clkp2" 55 respectively in order to advance or retard the  
16 timing edges in the signals  $S(n+1)'$  125 and  $S(n+1)''$  126.  
17 Logical "and" element 107 provides the logical function  
18 to produce the new signal  $S(n+1)'''$  127, which contains  
19 identical data to  $S(n+1)$  123 except that its rising and  
20 falling edges have been manipulated by the action of  
21 "clkp1" 53 and "clkp2" 55. Element 116 "inv" provides a  
22 logical inversion and element 115 "buf" provides a time  
23 delay buffer to match the delay introduced by "inv" of  
24 116. Subsequent modification is done by "Mux" 108 which  
25 outputs electronic signal ewave 25 as either normal or  
26 inverted copies of the signal  $S(n+1)'''$  under control of  
27 the pulse' 129 signal.

28

29 The synthesised input electronic signal ewave 25 is shown  
30 in Figure 5 showing rising edges 19, or falling edges 20  
31 that can be extended or reduced in time, of dTf 21 or dTr  
32 22 respectively, and energy removed from a "zero" by a  
33 short pulse of "one" 17, with duration dTl 23, and energy  
34 removed from a "one" by inserting a small pulse of "zero"

1 18, with duration dTh 24. However in alternative  
2 embodiments not all features of the method are required  
3 to be employed such that the edge time extension or  
4 reduction effects and/or the sub pulse insertion effects  
5 can be used to lesser degree, or completely removed. An  
6 associated reduction in the required apparatus to  
7 implement these solutions would then occur. Particular  
8 alternative embodiments can be achieved by:

9

- 10 1) Excluding Arm B 131 so that no edge modifications  
11 are possible. In this embodiment the signal  
12 S(n+1)''' 127 would be provided directly by the  
13 S(n+1) 123 signal;
- 14 2) Excluding within Arm B 131 elements 103 and 104,  
15 that control the rising edge of electronic signal  
16 ewave 25, or 105 and 106, that control the falling  
17 edge of electronic signal ewave 25. In this  
18 embodiment only rising or falling edge  
19 modifications respectively are possible and  
20 requires the signal S(n+1)' 125 or S(n+1)'' 126 to  
21 be replaced by S(n+1) 123, as appropriate;
- 22 3) Excluding within Arm C "clkp3" 57 and "buf" 109  
23 and replacing with "clk" 51 so that the rising  
24 edge of pulse' 129 is determined directly by  
25 "clk" 51 and is not controllable.
- 26 4) Excluding within Arm C "clkp4" 59 and "inv" 110  
27 and replacing with "clk" 51 so that the falling  
28 edge of pulse' 129 is determined directly by  
29 "clk" 51 and is not controllable.

30

31 In a further alternative embodiment the width of the sub  
32 pulses 17 and 18 can be applied independently to either  
33 the high or low signals within the data sequence. This is  
34 achieved by replacing the "xor" 113 with parallel "and"

1 and "nand" functions so producing two signals, namely  
2 "pulse\_h" and "pulse\_l". The "pulse\_h" and "pulse\_l"  
3 signals can then be used with a simple modification to  
4 Arm C 132 so as to accommodate the additional pulse  
5 selection via an additional selection element ("and" or  
6 "mux") that selects the signal pulse' 129 origin as  
7 being for a high (pulse\_h) or low (pulse\_l) data  
8 sequence. Additional clock phases would then be required  
9 in order to separately control the rising and falling  
10 edges of this additional selection of data dependant sub  
11 pulses.

12

13 Figure 11 more clearly shows the signal timing and  
14 logical relationships within the signal processing  
15 apparatus of Figure 10 and illustrates the scheme from  
16 the serial input signal "in" 1 to the electronic signal  
17 ewave 25.

18

19 Using the above signal processing scheme a time-domain or  
20 z-transform filter function is therefore effectively  
21 synthesised where the energy of any bit is a function of  
22 what has previously been sent. Expressing this in normal  
23 z-domain sampled data convention.

24

$$25 \quad Y(z) = X(z) * H(z)$$

26

27 where:

28        $Y(z)$  is the relative energy of the output  
29 sample

30        $X(z)$  is the relative energy of the input sample

31        $H(z)$  is the filter transfer function

32

$$33 \quad H(z) = A(1 - Bz^{-1})$$

34

1 where:

$$2 \quad A = (Ts - dTf - dTr)$$

**3**                    B = 1 / (Ts+dTf+dTr-dTl) for transmitted zeros

4 or

5 = 1 / (Ts-dTf-dTr-dTh) for transmitted ones

6

7 and where:

8 Ts= symbol bit period

13 (as defined in Figure 9)

14

15 It should be noted that this z-domain technique does not  
16 completely describe the action of the filter invention as  
17 it does not describe how energy can be shifted within one  
18 sample.

19

20 The described method and apparatus effectively provides a  
21 non linear (signal dependant) 1<sup>st</sup> order high frequency  
22 bandpass filter. By employing additional previous and  
23 future sample information through the incorporation of  
24 additional "latch" elements, and by using additional  
25 "xor" logical elements or similar structures, higher  
26 order high frequency band pass filters can readily be  
27 achieved.

28

29 It will be obvious to one skilled in the art that by  
30 altering the timing of the various clock pulses the  
31 adaptable signal processor can be converted so as to act  
32 as a low frequency bandpass filter, the order of which is  
33 dictated by the number of "latch", or similar elements,  
34 incorporated within the circuit.

1  
2 The apparatus if Figure 8 and 10 the signal processor  
3 uses no filter function to determine the  $S(n+1)'''$   
4 signal. However, this can readily be made data dependant  
5 and filters can be readily implemented by using a variety  
6 of logical schemes such as used to generate the pulse  
7 121.

8

9 Furthermore the apparatus of Figure 8 and 10 suggests  
10 that the signals are single bit digital lines. In  
11 practice they would most likely be differential signals  
12 with differential source coupled logic cells. These  
13 figures also suggest that the signals are only one bit  
14 wide but similar architecture using multiple bit wide  
15 parallel data lines could be used in high bandwidth  
16 systems with time-interleaving appropriately used for  
17 improved power trade-offs.

18

19 Aspects of the present invention described herein refer  
20 to a single channel communications system. However, in  
21 alternative embodiments, more channels can be employed,  
22 such as in a multi-core optical fibre or multi-strand  
23 twisted-pair e.g. CAT-5 cabling. The described aspects  
24 also refer to a communication system with a single  
25 channel with a single transmission signal present on the  
26 channel. However, in some embodiments, transmissions can  
27 be across one or more shared media channels using one or  
28 more signals such as, but not limited to, optical wave  
29 division multiplexing schemes (DWDM, CWDM), using  
30 multiple equalisers per signal.

31

32 The preferred embodiment of the present invention  
33 describes use mainly within the context of a fibre optic  
34 medium, however it is anticipated that it may be employed

1 with alternative transmission medium including, but not  
2 limited to, over air, optical fibre, printed circuit  
3 board or cable. Similarly aspects of the present  
4 invention may employ alternative transmission signal  
5 formats including, but not limited to, modulated, un-  
6 modulated, return to zero coding, non return to zero  
7 coding, encoded data, non encoded data, multi-level,  
8 binary, continuous or discontinuous, framed, burst or  
9 packet based or any combination of these. Furthermore,  
10 aspects of the present invention may employ alternative  
11 transmission technique including, but not limited to,  
12 electrical, electro-magnetic, magnetic or optical means.

13

14 The apparatus of aspects of the present invention present  
15 the transmitter 2 and the receiver 4 as two separate  
16 elements or components. Alternative embodiments that  
17 comprise multiple channel and bi-directional systems that  
18 incorporate transmitters and receiver that are joined or  
19 part joined within the same combined element or component  
20 of the system with the equaliser possibly additionally  
21 contained within.

22

23 The described apparatus further describes that the  
24 transmitter 2 is a distinct and separate element made up  
25 of two parts, the adaptable equaliser 7 and the optical  
26 source 8. However, alternative embodiments are envisaged  
27 where the transmitter element may also include a  
28 combination of additional separate, not necessarily  
29 distinct elements in any combination or form, such as a  
30 parallel to serial data converter, clock-data recovery  
31 unit, re-synchroniser, line driver, equaliser, optical  
32 source driver and the optical source itself.

33

1 Further alternative embodiments of aspects of the present  
2 invention include the communications system containing  
3 additional filters, transducers, amplifiers, sensors or  
4 other elements or components between multiple or single  
5 transmitters, receivers and medias. In addition the  
6 communication system could contain continuous or separate  
7 sections of media, separated by filters, transducers,  
8 sensors, transponders, transceivers, transmitters,  
9 receivers or other elements so as to break the media into  
10 one or more sections of not necessarily the same type of  
11 media.

12

13 The input signal 1, synthesis electronic signal ewave 25,  
14 optical wave owave 26 and apparatus presents a solution  
15 to a single binary on -off coding scheme. However, the  
16 principle can be applied to similar waves that are  
17 encoded in multiple levels such as a pulse amplitude  
18 modulation scheme (PAM encoding) and signal processing  
19 provided using a similar method.

20

21 In systems where the output amplitude can also be also  
22 directly influenced by the instantaneous amplitude of the  
23 ewave signal 25, additional equalisation can be applied  
24 using an amplitude modulation technique or the  
25 superposition of an additional pulse onto the ewave  
26 signal as appropriate to increase the energy of the  
27 signal in the frequencies of interest. A superposition  
28 technique such as analogue summation could be used.

29

30 Described herein is a method and apparatus for adapting  
31 an information carrying signal within of before an  
32 associated transmitter. This adaptation provides an  
33 efficient way of not only producing frequency dependent  
34 filters but also provides an effective means for the

1 equalisation of the information carrying signal. The  
2 transmitter effectively equalises by providing a pre-  
3 correction or compensation of the signal. As a result  
4 the transmitter based equalisation schemes described is  
5 capable of achieve higher performance than other prior  
6 art systems where equalisation takes place within the  
7 receiver or elsewhere in the channel. This effect is a  
8 direct result of the fact that this system can be  
9 designed so that the desired information carrying signal  
10 can be kept above the noise or other interference levels  
11 and hence can be more easily interpreted at the receiver.  
12 Furthermore, as the transmitter has an intrinsically  
13 accurate knowledge of what it is trying to transmit, and  
14 given information on what signal impairments exist in the  
15 system, more simplistic, intelligent, signal aware  
16 schemes such as those described above are possible.

17

18 A significant advantage of the described system is that  
19 it is very accurately controllable, has a fine  
20 resolution, a wide equalisation range, requires few high  
21 performance circuit elements to implement, requires less  
22 components or circuitry, requires little additional power  
23 and can be designed for low cost and high volume  
24 manufacturing than existing known schemes.

25

26 Additionally, because the synthesis technique is more  
27 controllable, this invention can provide more  
28 sophisticated equalisation or compensation for affects  
29 other simple bandwidth limitations such as complex non-  
30 linear and signal dependant ones. One practical use of  
31 this scheme is in high-speed fibre-optic systems where  
32 transmission distances are greatest and channel  
33 impairments are complex. Examples of such complex  
34 impairments include modal, chromatic and polarisation

1 dispersion and chirp of the optical fibre, saturation and  
2 scattering properties of the optical source and  
3 asymmetries and bandwidth limitations of the optical  
4 transmitter and receiver responses.

5

6 A further advantage of aspects of the present invention  
7 is that because both the eye closure 29 per length of  
8 media is improved and because the data jitter 28 per unit  
9 media is reduced, greater distance can be travelled  
10 before complete opto-electronic-opto signal regeneration  
11 or re-timing units are required. This greatly benefits  
12 the systems because it enables cheaper all optical  
13 systems to be made.

14

15 A yet further advantage is that more cost effective,  
16 lossy or dispersive media can be used and over greater  
17 distances in higher data rate applications. For example,  
18 twisted pair could be used where previously coaxial cable  
19 would have been required or multi-mode fibre where  
20 previously single-mode fibre was used.

21

22 Generally the method and apparatus of aspects of the  
23 present invention provide for the development and  
24 manufacture of higher performance communications systems,  
25 including optical ones, that are less expensive, less  
26 complex, less power demanding or more compact.

27

28 The foregoing description of the invention has been  
29 presented for purposes of illustration and description  
30 and is not intended to be exhaustive or to limit the  
31 invention to the precise form disclosed. The described  
32 embodiments were chosen and described in order to best  
33 explain the principles of the invention and its practical  
34 application to thereby enable others skilled in the art

1 to best utilise the invention in various embodiments and  
2 with various modifications as are suited to the  
3 particular use contemplated. Therefore, further  
4 modifications or improvements may be incorporated without  
5 departing from the scope of the invention as defined by  
6 the appended claims.